▪ Features

- Used with the DC006 to implement a direct memory access interface.
- Contains logic to request and gain control of the Q-bus.
- Allows four-word or multiple-word transfers.
- Contains bus receivers and drivers for direct connection to the computer bus.
- Uses external free-running clock and internally generates enable and disable clock controls.

▪ Description

The DC010 direct memory access (DMA), contained in a 20-pin dual-inline package (DIP), is a low-power Schottky device used primarily in a DMA device interface to perform the handshake operations required to request and gain control of the Q-bus. Once bus mastership has been established, the DC010 generates the required signals to perform a data-in (DATI) transfer, data-out (DATO) transfer, or a data-in/data-out (DATIO) transfer as selected by the control lines to the DC010. Four words or multiple words can be transferred before control of the bus is relinquished. Figure 1 is a simplified diagram of the logic contained on the DC010 chip. The signals in parenthesis connect internally.

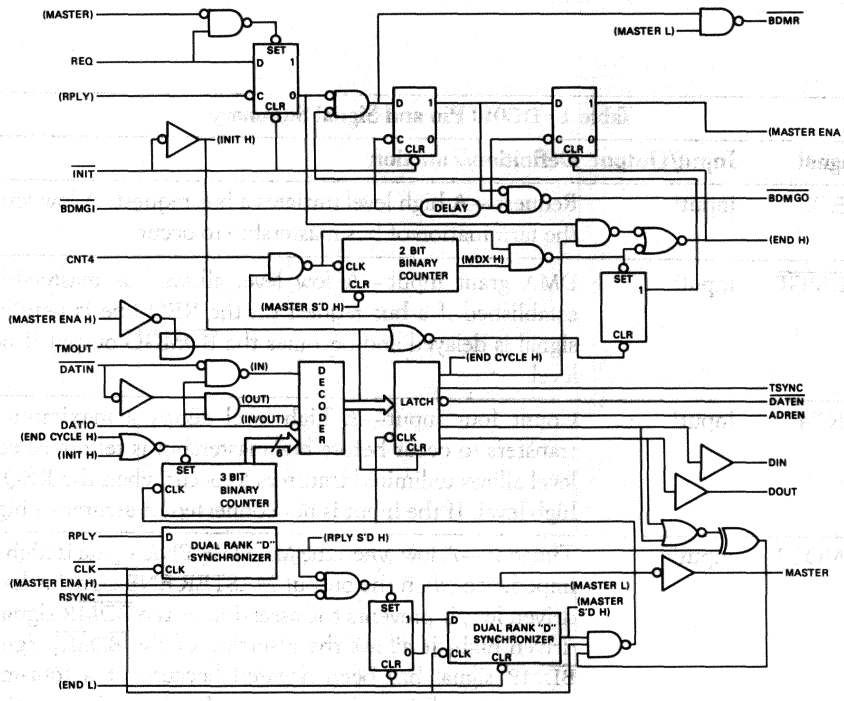


Figure 1 ▪ DC010 Simplified Logic Diagram

• Pin and Signal Descriptions

This section provides a brief description of the input and output signals and power and ground connections of the DC010 20-pin DIP. The pin assignments are identified in Figure 2 and the summarized in Table 1.

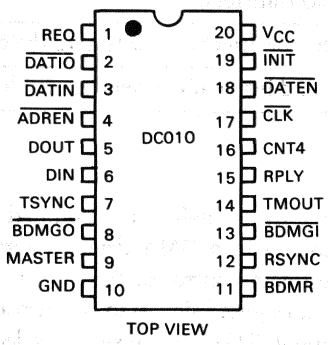


Figure 2 • DC010 Pin Assignments

Table 1 • DC010 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
1	REQ	input[1]	Request—A high level initiates a bus request. A low level allows the termination of bus mastership to occur.
13	$\overline{\text{BDMGI}}$	input[2]	DMA grant input—A low level allows bus mastership to be established if a bus request on the REQ line is pending. This signal is delayed and becomes the $\overline{\text{BDMGO}}$ output if not a low level.
16	CNT4	input[1]	Count four input—A high level allows a maximum of four transfers to occur before bus mastership is relinquished. A low level allows unlimited transfers to occur when the REQ line is a high level. If the input is not connected, it assumes a high state.
14	TMOUT	input[1,3]	Timeout—A low when the MASTER ENA signal is high. A high-impedance when the output MASTER ENB signal is low. When driven low, it prevents the assertion of the $\overline{\text{BDMR}}$ signal. When driven high, it allows the assertion of the $\overline{\text{BDMR}}$ signal if the $\overline{\text{BDMR}}$ signal has been negated because of a four-maximum transfer condition. A resistor and capacitor network can be connected to this pin to delay the assertion of the $\overline{\text{BDMR}}$ signal.

Pin	Signal	Input/Output	Definition/Function
3	$\overline{\text{DATIN}}$	input[1]	Data-in—Used with the DATIO signal to select the type of transfer as specified in Table 3.
2	$\overline{\text{DATIO}}$	input[1]	Data-in/Data-out—Used with the DATIN signal to select the type of transfer as specified in Table 3. If the input is not connected, it assumes a high state.
12	RSYNC	input[1]	Receive synchronize—Allows the device to become bus master according to the relationship of the following signals. $\overline{\text{RSYNC}} + \overline{\text{RPLY}} + \text{MASTER ENA} = \text{MASTER}$
17	$\overline{\text{CLK}}$	input_1	Clock—Used to generate all transfer timing sequences.
15	RPLY	input[1]	Reply—Enables or disables the clock signal and allows the device to become bus master according to the relationship of the following signals: $\overline{\text{RSYNC}} + \text{RPLY} + \text{MASTER ENA} = \text{MASTER}$
19	$\overline{\text{INIT}}$	input_1	Initialize—Used to initialize the logic so that the REQ signal will start a bus request transaction. A low level negates the $\overline{\text{BDMR}}$, MASTER, $\overline{\text{DATEN}}$, ADREN, RSYNC, DIN, and DOUT signals.
11	$\overline{\text{BDMR}}$	output[3]	DMA request—A low level indicates that the device is requesting bus mastership. May be connected directly to the Q-bus.
9	MASTER	output[1]	Master—Indicates that a device is bus master and that a transfer sequence is in progress.
8	$\overline{\text{BDMGO}}$	output[3]	DMA grant output—If no request is pending, this signal is the delayed output of the $\overline{\text{BDMGI}}$ input (pin 13). If a request is pending, this signal is not asserted. May be connected directly to the Q-bus.
7	TSYNC	output[1]	Transmit synchronize—Asserted by the device to indicate that a transfer is in progress.
18	$\overline{\text{DATEN}}$	output[1]	Data enable—Asserted to indicate that data may be transferred to the bus.
4	ADREN	output[1]	Address enable—Asserted to indicate that an address may be transferred to the bus.
6	DIN	output[1]	Data in—Asserted to indicate that the bus master device can accept data.
5	DOUT	output[1]	Data out—Asserted to indicate that the bus master device has transferred data to the bus.
20	V_{cc}	input	Voltage—Power supply dc voltage
10	GND	input	Ground—Common ground connection

[1]TTL level
[2]high-impedance
[3]open-collector

Functional Description

The DATIN and DATIO are TTL input levels that select the type of DMA transfer that will occur. Table 2 lists the input levels and the transfer selected.

Table 2 • DC010 Transfer Selection

Inputs Levels* DATIN	DATIO	Transfer Type
X	L	DATIO
L	H	DATI
H	H	DATO

*L = TTL low, H = TTL high, X = TTL low or high

• Application Information

Refer to the *Chipkit Users Manual LSI-11 Bus Interface Chips* (document no. EJ-01387-92) for general application information. The Q-bus is an LSI-11 bus.

• Specifications

The mechanical, electrical, and environmental characteristics and specifications for the DC010 are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Operating temperature (T_A): 0°C to 70°C
- Supply voltage (V_{CC}): 5.0 V ±5%

Mechanical Configuration

The physical dimensions of the DC010 20-pin DIP are contained in Appendix E. The materials and construction of the DIP are defined in Digital Specification A-PS-1900002-GS.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Supply voltage (V_{CC}): 7.0 V
- Input voltage (V_I): 5.5 V
- Operating temperature (T_A): 0°C to 70°C (32°F to 158°F)
- Storage temperature (T_S): –65°C to 150°C (–149°F to 302°F)

Recommended Operating Conditions

- Supply voltage (V_{CC}): 4.75 V (minimum), 5.0 V (normal), 5.25 V (maximum)
- Supply current (I_{CC}): 160 mA (maximum)
- Free-air temperature: 0°C to 70°C (32 F to 158°F)
- Relative humidity: 10% to 95% (noncondensing)

dc Electrical Characteristics

The dc electrical parameters of the DC010 for the operating voltage and temperature ranges specified are listed in Table 3. Refer to Appendix C for the test circuit configurations referenced in the table.

Table 3 • DC010 Input and Output Parameters

Parameter	Symbol	Test Condition	Requirements Min	Requirements Max	Units	Test Circuit
High-level input voltage	V_{IH}		2.0		V[1]	C1,C2
		$V_{CC}=4.75$	1.53		V[2,3]	
		$V_{CC}=5.25$	1.70		V[1]	
Low-level input voltage	V_{IL}			0.8	V[1]	C1,C2
		$V_{CC}=4.75$		1.30	V[2,3]	
		$V_{CC}=5.25$		1.47	V[2,3]	
Input clamp voltage	V_I	$V_{CC}=$ open, $I_I=-18$ ma	—	−1.2	V[1,2,3]	C3
High-level output voltage	V_{OH}	$V_{CC}=4.75$, $I_O=-1.0$ mA	2.7	—	V[1]	C1
Low-level output voltage	V_{OL}	$V_{CC}=4.75$ V				C2
		$I_O=8$ mA	—	0.5	V[1]	
		$I_O=70$ mA	—	0.8	V[3,4]	
Input current at maximum input voltage	I_I	$V_{CC}=5.25$ V	—	1.0	mA[5]	C4
		$V_I=5.5$ V	—	1.5	mA[6]	
High-level input current	I_{IH}	$V_{CC}=5.25$ V[5]				C4
		$V_I=2.7$ V	—	50	μA	
		$V_I=2.7$ V[6]	—	300	μA	
		$V_I=3.8$ V	—	40	μA[2]	
		$V_I=3.8$ V	—	65	μA[3]	
Low-level input current	I_{IL}	$V_I=0.5$ V[5]				C5
		$V_{CC}=5.25$ V	—	−1.4	mA	
		$V_{CC}=5.25$ V	—	−2.0	mA	
		$V_{CC}=0$–5.25 V	—	−10	μA[2]	
		$V_{CC}=0$–5.25 V	—	−10	μA[3]	

Parameter	Symbol	Test Condition	Requirements Min	Max	Units	Test Circuit
Output leakage	I_{OH}	V_{cc}=4.75 V V_o=5.25 V		25	µA[4]	C1
Short-circuit output current	I_{os}	V_{cc}=5.25 V[7]	-15	-60	mA[1]	C6
Supply current	I_{cc}	V_{cc}=5.25 V	125	160	mA	C7

[1]TTL input
[2]high-impedance input
[3]high-impedance (Schmidt) input, open-collector output
[4]open-collector output
[5]except pin 16 and pin 2
[6]pin 16 and pin 2
[7]Not more than one output shall be short circuited at a time and the duration of the short must not exceed 1 second.

ac Electrical Characteristics

The input and output signal timing for the DC010 is shown in Figures 3 through 7. The setup time, pulse-widths, and switching characteristics referenced in the timing diagrams are listed in Table 4. Table 5 lists the signal propagation delays also referenced in the timing diagrams. Figure 8 shows the load circuits used for measuring for the open-collector and TTL outputs. Refer to Appendix D for the input and output voltage waveforms used for measuring the signal propagation delays.

Figure 3 shows the signal timing required for the DMA bus-request and bus-grant logic. Figure 4 shows the signal timing required for one data-in (DIN) transfer to the DMA interface. The signal timing required for one data-out transfer is shown in Figure 5. Figure 6 shows the signal timing required for multiple-data transfers in and out of the DMA interface. The signal timing for the timeout sequence is shown in Figure 7. The values of the resistor (Rx) and capacitor (Cx) used in the timeout circuit shown in Figure 9 are selected for the proper delay for the next DMA request from the interface. The delay circuit connects to pin 14 (TMOUT).

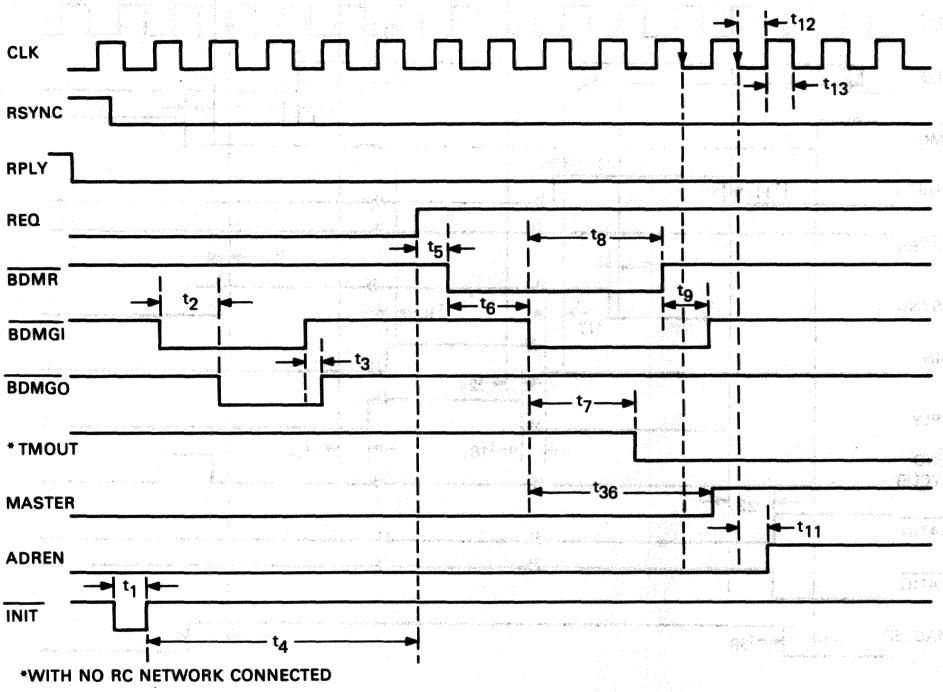


Figure 3 • DC010 DMA Bus Request and Grant Signal Timing Sequence

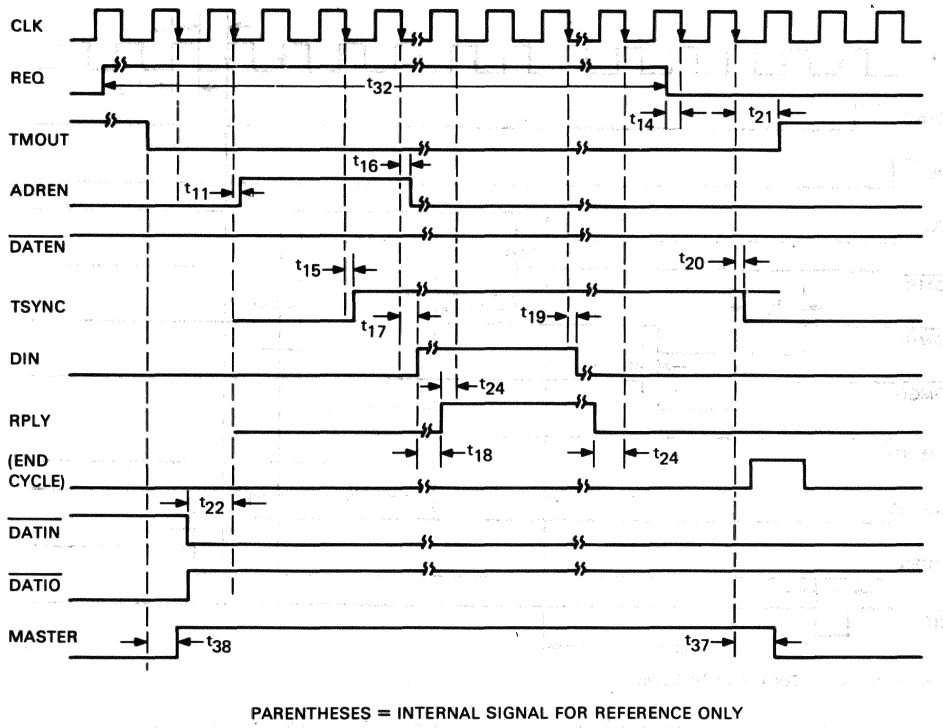
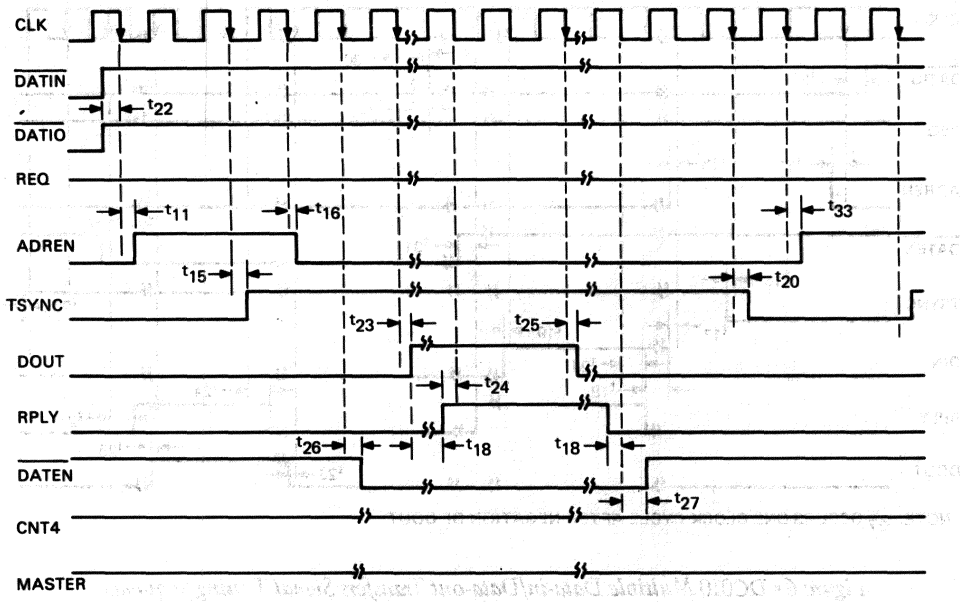


Figure 4 • DC010 One Data-in Transfer Signal Timing Sequence



NOTE: t_{27} OCCURS ONE CLOCK CYCLE AFTER NEGATION OF DOUT

Figure 5 • DC010 Data-out Transfer Signal Timing Sequence

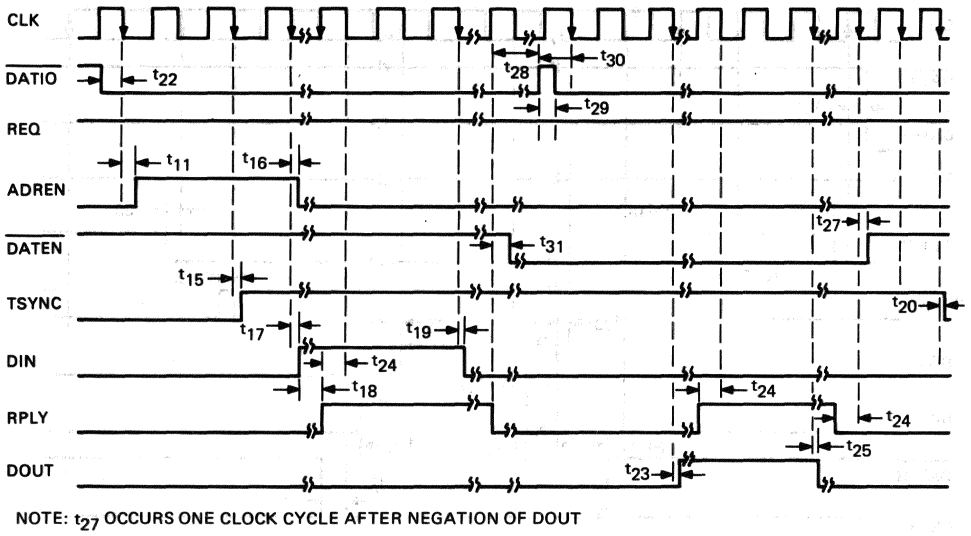


Figure 6 ▪ DC010 Multiple Data-in/Data-out Transfers Signal Timing Sequence

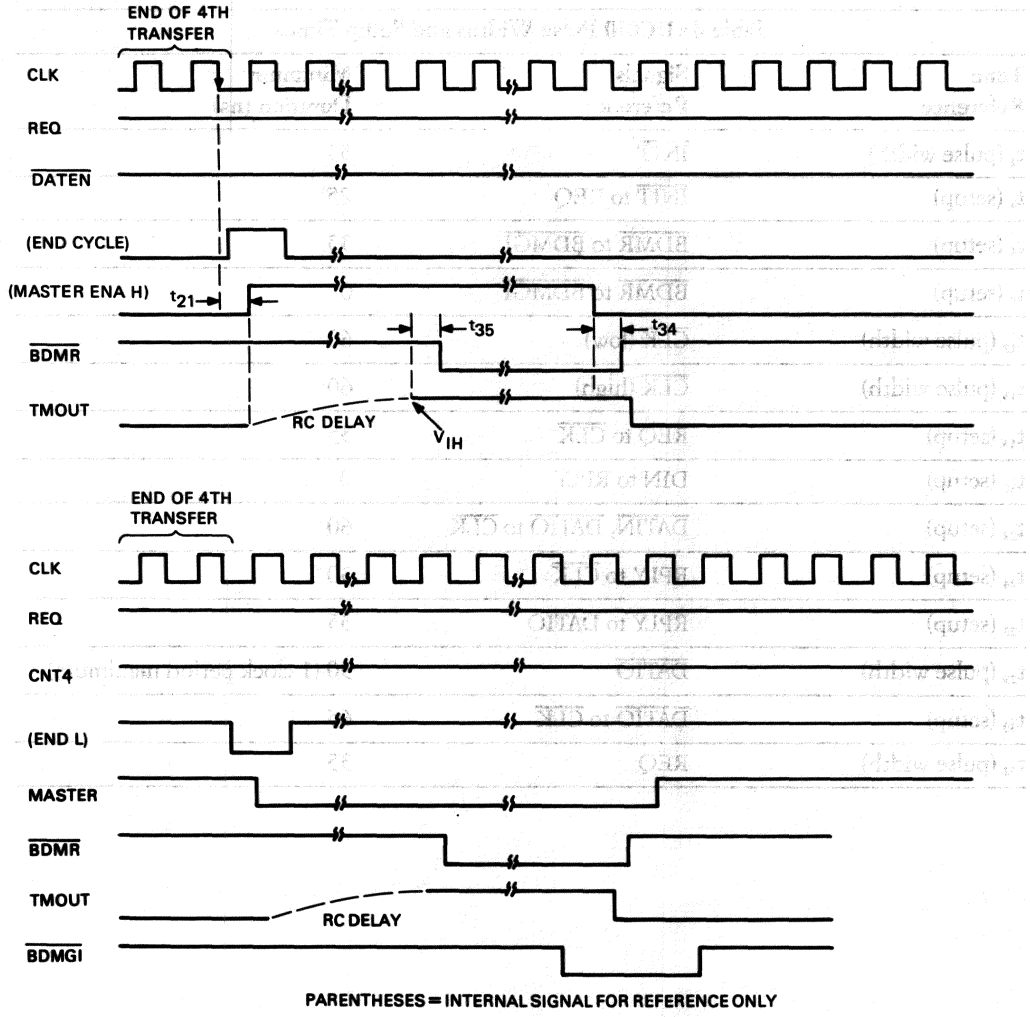


Figure 7 • DC010 Timeout Signal Timing Sequence

Table 4 • DC010 Pulse Widths and Setup Times

Time Reference	Signals Reference	Minimum Duration (ns)
t_1 (pulse width)	$\overline{\text{INIT}}$	35
t_4 (setup)	$\overline{\text{INIT}}$ to REQ	25
t_6 (setup)	$\overline{\text{BDMR}}$ to $\overline{\text{BDMGI}}$	35
t_9 (setup)	$\overline{\text{BDMR}}$ to $\overline{\text{BDMGI}}$	0
t_{12} (pulse width)	$\overline{\text{CLK}}$ (low)	60
t_{13} (pulse width)	$\overline{\text{CLK}}$ (high)	60
t_{14} (setup)	REQ to $\overline{\text{CLK}}$	35
t_{18} (setup)	DIN to RPLY	0
t_{22} (setup)	$\overline{\text{DATIN}}$, $\overline{\text{DATIO}}$ to $\overline{\text{CLK}}$	60
t_{24} (setup)	RPLY to $\overline{\text{CLK}}$	30
t_{28} (setup)	RPLY to $\overline{\text{DATIO}}$	35
t_{29} (pulse width)	$\overline{\text{DATIO}}$	30 (1 clock period maximum)
t_{30} (setup)	$\overline{\text{DATIO}}$ to $\overline{\text{CLK}}$	65
t_{32} (pulse width)	REQ	35

Table 5 • DC010 Signal Propagation Delays

Timing Reference	Input Signal (Transition)	Output Signal (Transition)	Test Condition[1,2]	Propagation Delay (ns) Min.	Max.
t_2	$\overline{\text{BDMGI}}$ (H-L)	$\overline{\text{BDMGO}}$ (H-L)	Load A	95	220
t_3	$\overline{\text{BDMGI}}$ (L-H)	$\overline{\text{BDMGO}}$ (L-H)	Load A	15	60
t_5	REQ (L-H)	$\overline{\text{BDMR}}$ (H-L)	Load A	25	70
t_7	$\overline{\text{BDMGI}}$ (H-L)	TMOUT (H-L)	Load A	85	230
t_8	$\overline{\text{BDMGI}}$ (H-L)	$\overline{\text{BDMR}}$ (L-H)	Load A	117	306
t_{11}[2]	$\overline{\text{CLK}}$ (H-L)	ADREN (L-H)	Load B	15	60
t_{15}	$\overline{\text{CLK}}$ (H-L)	TSYNC (L-H)	Load B	18	60[3]
t_{16}	$\overline{\text{CLK}}$ (H-L)	ADREN (H-L)	Load B	20	65[3]
t_{17}	$\overline{\text{CLK}}$ (H-L)	DIN (L-H)	Load B	18	60[3]
t_{19}	$\overline{\text{CLK}}$ (H-L)	$\overline{\text{DIN}}$ (H-L)	Load B	18	60
t_{20}	$\overline{\text{CLK}}$ (H-L)	TSYNC (H-L)	Load B	18	60
t_{21}	$\overline{\text{CLK}}$ (H-L)	TMOUT (L-H)	Load B	30	90
t_{23}	$\overline{\text{CLK}}$ (H-L)	DOUT (L-H)	Load B	60	175
t_{25}	$\overline{\text{CLK}}$ (H-L)	DOUT (H-L)	Load B	20	65[3]
t_{26}	CLK (H-L)	$\overline{\text{DATEN}}$ (H-L)	Load B	20	65[3]
t_{27}	$\overline{\text{CLK}}$ (H-L)	$\overline{\text{DATEN}}$ (L-H)	Load B	20	65[3]
t_{31}	RPLY (H-L)	$\overline{\text{DATEN}}$ (H-L)	Load B	20	65
t_{33}[2]	$\overline{\text{CLK}}$ (H-L)	ADREN (L-H)	Load B	18	60
t_{35}	TMOUT (L-H)	$\overline{\text{BDMR}}$ (H-L)	Load B	20	75
t_{36}	$\overline{\text{BDMGI}}$ (H-L)	MASTER (L-H)	Load B	90	242
t_{37}	$\overline{\text{CLK}}$ (H-L)	MASTER (H-L)	Load B	18	66
t_{38}	RSYNC (H-L)	MASTER (L-H)	Load B	10	58

[1]See Figure 8 for output load circuit configurations.

[2]t_{11} represents the first time ADREN is asserted. t_{33} represents the subsequent assertion of ADREN.

[3]These propagation delays meet the following requirements:

t_{15} to $t_{16} \leq 10$ ns t_{25} to $t_{27} \leq 20$ ns

t_{15} to $t_{17} \leq 10$ ns t_{23} to $t_{26} \leq 40$ ns

t_{16} to $t_{26} \leq 10$ ns t_8 to $t_{36} \leq 27$ ns

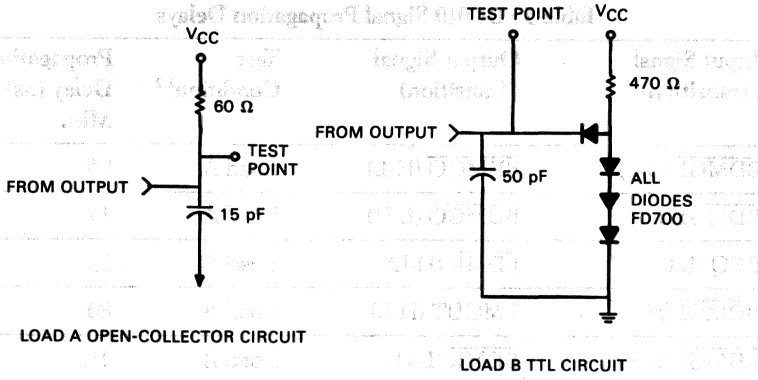


Figure 8 • DC010 Output Load Circuits

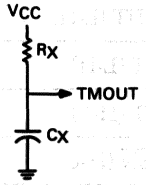


Figure 9 • DC010 Timeout Delay Circuit